R E M A R K S

Careful review and examination of the subject application are noted and appreciated. Applicant's representative thanks Examiner Chang for the indication of allowable subject matter.

SUPPORT FOR CLAIM AMENDMENTS

The claims have been amended for consistency. Support for the amendments to the claims ban be found in the claims as originally filed. As such, no new matter has been introduced.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1, 14 and 27 under 35 U.S.C. §102(e) as being anticipated by Field et al. (U.S. Patent No. 6,778,529; hereinafter Field) is respectfully traversed and should be withdrawn.

Field is directed to a synchronous switch and method for a telecommunications node (Title of Field).

In contrast, the present invention provides a time-slot interchanger for interchanging the order of subframes of data within an input data frame comprising: (i) a global frame clock, (ii) an interchange random access memory receiving the input data frame, out of alignment with the global frame clock, at an input, (iii) a write address generator which addresses the random access memory to write subframes, out of alignment with the global frame clock, in a received order, and (iv) a read address generator which

addresses the random access memory to read subframes in interchanged order and aligned to the global frame clock. Claims 14 and 27 include similar limitations.

Assuming, *arguendo*, (i) the switching memory 656 of Field is similar to the presently claimed interchange random access memory and (ii) the frame pulse of Field is similar to the presently claimed global frame clock (as suggested in lines 6-9 of section 2 on page 2 of the Office Action and for which Applicant's representative does not necessarily agree), Field does not appear to disclose or suggest each and every element of the presently claimed invention, arranged as in the claims. Specifically, the switching memory 656 of Field does not appear to **receive an input data frame, out of alignment with the global frame clock, at an input**, as presently claimed. In particular, the text of Field cited by the Office Action reads:

> FIG. 32 illustrates a deterministic pattern for accessing the switching memory 656 in accordance with one embodiment of the present invention. In this embodiment, each 125 microsecond frame period is divided into 256 subframes, each of which includes 64 cycles. **The switch and line cards are synchronized to this 125 microsecond frame pulse** which in turn is derived from the systems clock. **This synchronization at this level minimizes the amount of interface logic required for the system.** A repeated schedule of RAM accesses are performed each subframe consisting of 30 egress reads followed by 30 egress writes. As previously described, the controller 552 provides the base addresses prior to each read and write operation. The switching memory 652 then either performs a linear read or write burst transfer of the two words starting at

> that address (column 32, lines 12-36 of Field, emphasis added).

No where in the cited text does Field disclose or suggest receiving the input data frame, out of alignment with the frame pulse, at an input of the switching memory 656.

Furthermore, FIGS. 33 and 34 and column 32, line 27 through column 33, line 18 of Field (which are cited by the Office Action in the last 5 lines on page 2 and lines 1-4 on page 3) appear silent regarding receiving the input data frame, out of alignment with the frame pulse, at an input of the switching memory 656. Since the switch (including the switching memory 656) and line cards of Field are synchronized to the frame pulse and Field appears silent regarding receiving the input data frame, out of alignment with the frame pulse, at an input of the switching memory 656, it follows that Field does not disclose or suggest an interchange random access memory receiving the input data frame, out of alignment with the global frame clock, at an input, as presently claimed. Therefore, Field does disclose or suggest each and every element of the presently claimed invention, arranged as in the claims. As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Furthermore, Field identifies the switching memory 656 as being part of a high capacity ATM switch card (see column 4, lines 26-29 and column 30, lines 7-17 of Field). The Office Action does not present any objective evidence or convincing line of reasoning

why a person of ordinary skill in the field of the present invention would consider the ATM switch of Field to be the same as a time slot interchanger comprising an interchange random access memory as presently claimed. Therefore, the Office Action does not meet the Office's burden to factually establish a *prima facie* case of anticipation by showing that there is "no difference between the claimed invention and the reference disclosure, as viewed by a person of ordinary skill in the field of the invention." As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claims 13 and 26 under 35 U.S.C. §103 as being unpatentable over Field in view of Böttle et al. (U.S. Patent No. 5,303,077; hereinafter Böttle) is respectfully traversed and should be withdrawn.

Claim 26 depends directly from claim 14 which is believed to be allowable. As such, claim 26 is fully patentable over the cited references and the rejection should be withdrawn.

Claim 13 recites a time-slot interchanger as claimed in claim 1 and, therefore, incorporates by reference the limitations of claim 1. For the reasons provide above, Field does not teach or suggest a time-slot interchanger as claimed in claim 1. Furthermore, the Office Action states that Field does not expressly disclose at least one switch of at least one stage comprising a

time-slot interchanger (see lines 3-6 is section 3 on page 3 of the Office Action).

Böttle does not cure the deficiencies of Field. Specifically, the Office Action fails to present objective evidence or a convincing line of reasoning that Böttle teaches or suggests a time-slot interchanger meeting the specific limitations recited in claim 1. In particular, Böttle appears to be silent regarding a structure of the time-slot interchangers 121, ..., 12n. Since Böttle is silent regarding the structure of the time-slot interchangers, it follows that Böttle does not teach or suggest a time-slot interchanger comprising (i) a global frame clock, (ii) an interchange random access memory receiving the input data frame, out of alignment with the global frame clock, at an input, (iii) a write address generator which addresses the random access memory to write subframes, out of alignment with the global frame clock, in a received order and (iv) a read address generator which addresses the random access memory to read subframes in interchanged order and align to the global frame clock, as presently claimed. Thus, the Office Action fails to meet the Office's burden to show that the combination of Field and Böttle teaches each and every element of the presently claimed invention. Therefore, the Office Action fails to factually establish a *prima facie* case of obviousness (MPEP §2142). As such, the presently claimed invention is fully patentable over the cited references and the rejection should be withdrawn.

Furthermore, the Office Action appears to have used improper hindsight-based analysis to select the cited references. Specifically, the Office Action appears to have used claims 13 and 26 as templates for selecting the cited references. The Federal Circuit has prohibited the use of hindsight in the production of a *prima facie* case of obviousness. Furthermore, the conclusory statement that the suggestion/motivation to do so would have been to accommodate a multi-stage digital cross-connect switch and to take advantage of the time-clot interchanger and the space switch capable of the subframe interchange in claims 13 and 26 fails to cite the specific understanding or knowledge in the art or the specific passages within the cited references which provide such a suggestion or motivation. Therefore, the Office Action fails to meet the Office's burden to factually establish a *prima facie* of obviousness (MPEP §2142). As such, the presently claimed invention is fully patentable over the cited references and the rejection should be withdrawn.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative at 586-498-0670 should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge Deposit Account No. 12-2252.

Respectfully submitted,

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